ABSTRACT

0023 A method for forming an offset spacer adjacent a CMOS gate structure with improved critical dimension control including providing a substrate that has a gate structure; forming at least one oxide layer over the substrate; forming at least one nitride layer over the at least one oxide layer; dry etching the at least one nitride layer in a first dry etching process to expose a first portion of the at least one oxide layer; carrying out a wet etching process to remove the first portion of the at least one oxide layer; and, dry etching the at least one nitride layer in a second dry etching process to remove the at least one nitride layer leaving a second portion of the at least one oxide layer to form an oxide offset spacer along sidewalls of the gate structure.